

A Circuit for Improving Clock Rates in High Speed Electronic Circuits Using Feedback Based Flip-Flops

Abstract

A flip-flop circuit for enhancing clock rates in high speed electronic circuits, the flip-flop circuit having an input terminal, an output terminal, and a third terminal that controls the flow of signal from the input terminal to the output terminal, comprising: two latches arranged in a master-slave configuration such that the input terminal of the first latch is also the input terminal of the flip-flop and the output terminal of the second latch is also the output terminal of the flip-flop; and at least one feedback path that adds signal to the input of the flip-flop from one of the outputs of the two latches.

Patent application no. 44/MUM/2014