Single Event Soft Error (SE) Tolerant Latch

Embodiments herein provides the latch including a first circuit module with an one p-channel transistor and two n-channel transistor (1P-2N) or two p-channel transistor and one n-channel transistor (2P-1N). A second circuit module is coupled to the first circuit module. The second circuit module includes the 1P-2N or the 2P-1N. An auxiliary module includes one of: a back-to-back inverter element, a 3-input C-element, and one of: a clocked 1P-2N or a clocked 2P-1N. A clocked circuit module includes the 1P-2N or the 2P-1N. The first circuit module and the second circuit module are coupled to the clocked circuit module. The latch writes data when the latch is operated in a transparent mode. The latch stores data when the latch is operated in a hold mode.

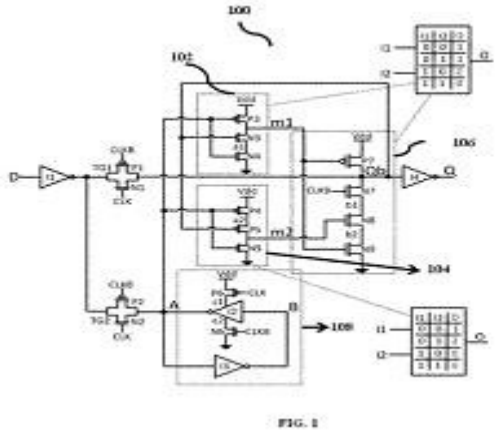

FIG. 1

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