Electronic and Optoelectronic Devices using 2D van der Waals Materials

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Outline

- Introduction to 2D van der Waals Materials

- Electronic Transistors
  - Contact Resistance
  - P-type Doping for P-FETs and PN junctions

- Optoelectronic Photodetectors
  - ReS$_2$ Gated Photodetectors
  - ReS$_2$/WSe$_2$ Heterojunction PN Photodiodes
  - WSe$_2$ N-P-N Bipolar Phototransistors

- Summary and Acknowledgements
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2D Materials and Applications

- An explosion of 2D materials in the post-graphene era
- Wide array of applications from sensing to spintronics


2D Materials and Device Research (2013- present)

Electronic Devices:
- Contact Resistance, Doping, Noise

Optoelectronics:
- Plasmonics
- Photodetection

Device modeling:
- DFT Simulations and NEGF Transport

2D Mat. & Devices

Nature 2D Materials and Applications (2017)
Nanoscale (2018)

IEEE TED (2018)

ACS Nano (2016)
APL (2014)

Sc. Reports (2017)

ACS Applied Materials and Interfaces (2016)


ACS Applied Materials and Interfaces (2018)
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Transistor Scaling

- High performance options
  - Germanium, III-V channels

- Low power roadmap
  - GAA, T-FET, NC-FET, 2D-FET
Contact Resistance in MoS$_2$ Transistors

- Demonstration of Fermi-level pinning in MoS$_2$
- Lowering of contact resistance through interfacial TiO$_2$

**Au and Pd Contact Barrier Heights**

- TiO$_2$ contact Interfacial Layer

DRC ('14), APL ('14)

ACS Appl. Materials & Interfaces ('15)
MoS₂ P-FETs and PN Diodes

- **P-type doping** of MoS₂ using CMOS processing
- **Reversible hysteresis inversion** in MoS₂ transistors

**ACSM Nano ('16)**

**P+ Si (Gate)**

**Contact**

**P-MoS₂**

**N-MoS₂**

300 nm SiO₂

**P+ Si (Gate)**

**Contact**

**p-MoS₂**

**n-MoS₂**

300 nm SiO₂

**SiO₂**

**ΔV_TH (V)**

Nature 2D Materials & Appl. ('17) (Denmark Tech. Univ.)
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Optoelectronics using 2D Materials

- High absorption with variable bandgap → broad spectral range
- Transparent (thin) and bendable → flexible optical displays/sensors/wearables, transparent photo-voltaics
- Atomically sharp p-n junctions → efficient photo-generation, carrier separation and low dark current
- Naturally passivated and high speed → facile integration with optical communication links

2D Photodetectors: Performance Metrics

- Fast, High Gain

![Graph showing performance metrics for various 2D photodetectors](image)

- Responsivity vs. Response time
- Trade-off between speed and responsivity

- Photoconductive Gain (G):\[ G = \frac{\tau_{\text{lifetime}}}{\tau_{\text{transit}}} \]

- Trap results in Photoconductive Gain (G)

- Speed: \[ \propto \frac{1}{\tau_{\text{lifetime}}} \]

Multilayer ReS$_2$ Photodetectors

Supported transistor

Suspended transistor

More traps, good gate control

Less traps, poor gate control

ACS Appl. Materials & Interfaces ('18)
Tunable Responsivity and Speed Performance

- **High Speed**: amongst fastest 2D semiconductor photodetectors
- **High Gain**: tunable with gate bias
ReS$_2$-WSe$_2$ Heterojunction PN Diodes

- Fabricated using a dry flake transfer technique
- Type II Heterojunction PN Diode

- Electrode 1
- Electrode 2

$E_G = 1.5$ eV
$\Delta E_C = 0.68$ eV
$\chi = 4.68$ eV
$E_F$
$E_V$

$\Delta E_V = 0.98$ eV
$E_G = 1.2$ eV
$\chi = 4.0$ eV

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Fastest 2D semiconductor photodetector in visible range with high gain
Photovoltaic Effect

- Best reported PV performance
- "All-2D" photodetector for easy integration with flexible substrates

![Graph showing I-V characteristics](image)

- $E_G = 1.5 \text{ eV}$
- $E_G = 1.2 \text{ eV}$

![Diagram of photovoltaic device](image)
Electrostatically doped bipolar (NPN/PNP) device
“All-2D” architecture for easy integration with flexible devices
NPN Transistor \rightarrow NNN Resistor

- \( V_{CE} \)
- \( G_{C} \) (2 V)
- \( G_{B} \) (-3 to 3 V)
- \( G_{E} \) (2 V)
- \( V_{GB} = -3 \text{ V} \) (n-p-n)
- \( V_{GB} = 3 \text{ V} \) (n-n-n)

Graph:
- \( I_{C} (\mu A) \) vs. \( V_{CE} (V) \)

Data points:
- 0.0
- 0.5
- 1.0
- 1.5
- 2.0

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Photo-amplification in NPN Mode

- n-p-n BJT configuration
- 2x gain vs forward biased pn
- 25x gain vs reverse biased pn

![Diagram showing n-p-n BJT configuration with voltage levels and photocurrent curves.](image)

- $V_{CE}$
- $G_C$
- $G_B$
- $G_E$

**Photocurrent**

- $I_{ph}$ vs $V_{GB}$

- $V_{GE} = 2$ V
- $V_{GE} = -2$ V
- $V_{GE}$ range: -3 to 3 V

- $V_{CE}$ range: 2 V, -2 V/2 V

- $I_{ph}$ range: 0 to 800 nA

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### Summary

1. 2D van der Waals semiconductors help extend low power transistor roadmap
   - Low contact resistance and selective, stable n/p doping are critical requirements

2. 2D vdW materials can also enable high performance flexible optoelectronic applications
   - Large area growth and all-2D architecture needed
Acknowledgments
Backup
Fabrication Process Flow: Supported Transistor

1. Mechanically exfoliate 2D material
2. Coat with photoresist
3. Lithography (Optical or e-beam)
4. Photoresist development
5. Metallization (evaporation)
6. Liftoff
2D Material
Photoresist
**p** + Si
Metal
SiO$_2$
**p+ Si**
Lithography

**Fabrication Process Flow: Suspended Transistor**

Coat with photoresist layer 1
Mechanically exfoliate 2D material
Coat with photoresist layer 2
Lithography (Optical or e-beam)
Photoresist development
Metallization (sputter)
Liftoff

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Photocurrent Setup

- Laser: 633 nm
- Acousto-Optic Modulator
- Function Generator (1 - 100 KHz)
- Lock-in Amplifier
- Current Preamp
- Source
- Drain
- Piezoelectric Stage
- \( V_g \)
- \( V_{bias} \)
- Long working distance microscope objective
- Vacuum box

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Transfer Curves under Illumination

Evidence of PC and PG effects
Photocurrent Spatial Scans

- Photocurrent Map (nA)

- Suspended ReS$_2$ to Source

- Drain

- Laser: 633 nm

- Acousto-Optic Modulator

- Function Generator (1 - 100 KHz)

- Lock-in Amplifier

- Current Preamp

- Piezoelectric Stage

- Long working distance microscope objective

- Source to Drain

- $V_g$

- $V_{bias}$
Photocurrent Spatial Scans

\[ R = \frac{I_{ph}}{P} \]
\[ \Rightarrow I_{ph} \propto P^{0.31} \]

\[ I_{ph} \propto P^\eta, \eta < 1 \] indicates the presence of traps.
Types of Traps

*Intrinsic* bulk traps in the semiconductor

*Extrinsic* interface traps at the semiconductor/oxide interface

**M. Buscema et al., Chem. Soc. Rev. (2015)**

**B. Mukherjee et al., IEEE DRC (2017)**
Low Frequency Dynamic Photoresponse

Decreasing effective trap density and increasing speed

(a) Supported ReS$_2$ Device
$V_G = 0$ V, $V_D = 1$ V

(b) Suspended ReS$_2$ Device
$V_G = -60$ V, $V_D = 0.5$ V

(c) Suspended ReS$_2$ Device
$V_G = 60$ V, $V_D = 0.5$ V

(d) Supported ReS$_2$ Device
$V_G = 80$ V, $V_D = 1$ V

(e) Photocurrent (nA)
$T_{ex} = 10$ minute
$\tau_1 \sim 367$ s

(f) Photocurrent (nA)
$T_{ex} = 10$ minutes
$\tau_1 \sim 287$ s

(g) Photocurrent (nA)
$T_{ex} = 10$ minutes
$\tau_1 \sim 261$ s

(h) Photocurrent (nA)
$T_{ex} = 5$ minute

(i) Photocurrent (nA)
$T_{ex} = 15$ seconds

(j) Photocurrent (nA)
$T_{ex} = 15$ seconds

(k) Photocurrent (nA)
$T_{ex} = 15$ seconds

(l) Photocurrent (nA)
$T_{ex} = 15$ seconds

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Gate bias and device architecture can be used to move between PG (slow) and PC (fast) switching.
Effect of Traps

\[ N_{Total} = \frac{\Delta V_{Th} C_G}{q} \sim 3.78 \times 10^{12} \text{ cm}^{-2} \]

\[ N_{IT} \sim \frac{0.1 \times (\Delta SS \cdot C_G)}{kT \ln(10)} \sim 0.78 \times 10^{12} \text{ cm}^{-2} \]

\[ \Delta V_{Th} \sim 50 \text{ V} \]

\[ \Delta SS \sim 6.4 \text{ V/decade} \]

![Graph showing the effect of traps on device behavior](image)

(a) Impact of effective trap density

- **PC**
- **PG**
- **Supported ReS\(_2\)**
- **Suspended ReS\(_2\)**
- **Guide to the eye**

- \( R \sim 2 \) (Effect of Architecture)
- \( R \sim 0.5 \)
- \( R \sim 8 \) (Effect of Gate Bias)

- \( N_{IT} \)
- \( N_{BT} \)
- \( N_{IT} + N_{BT} \)

ref: 10.1021/acsami.8b11248
Fabrication Process Steps

1. Fabricate gate electrodes
2. Transfer hBN
3. Transfer WSe$_2$
4. Fabricate E/C electrodes
5. p+ Si/SiO$_2$
Characterization of pn diode configuration

\[ V_{GC} = -2 \text{ V} \quad V_{GE} = 2 \text{ V} \]

-2 to 2 V
Floating
2 V

\[ I_C (A) \quad V_{CE} (V) \]
- Rectification with gate bias in all configurations.
- Gate tunable rectification ratio \( > 10^4 \).

Rectification Ratio - 1 V

\[ \text{Rectification Ratio} = \frac{I_{fb}}{I_{rb}} \]

pn diode
Effect of $V_{GB}$ on electrical response

$V_{CE}$

$V_{GB} = -3$ V (n-p-n)

$V_{GB} = 3$ V (n-n-n)

$I_C$ (μA)

$V_{CE}$ (V)
Photoresponse of pn diode

Photoresponse of pn diode

Increasing Intensity

Photovoltaic Effect

$V_{CE}$

$GND$

$G_C$

$G_B$

$G_E$

$I_C$ (A)

$V_{CE}$ (V)

Dark

$10^{-11}$ $10^{-9}$ $10^{-7}$ $10^{-5}$
Photovoltaic response of pn diode

Short-circuit Current

Open-circuit Voltage

I_{sc} (nA)

V_{GC} (V)

V_{CE} (V)

V_{oc} (mV)

V_{oc}
Figure 4: Photoresponse characteristics. I-V characteristics under illumination (a). Responsivity (b) and Detectivity (d) under illumination at different reverse bias voltages. Power law for the Responsivity (c) and photo-amplification with laser power (e).
Figure 5: Photovoltaic effect - Fourth quadrant plot (a), Power generated (b), Fill factor at various laser powers (c). Variation of ISC (d) and VOC at various back-gate voltages. Schematic of the photogeneration (e).