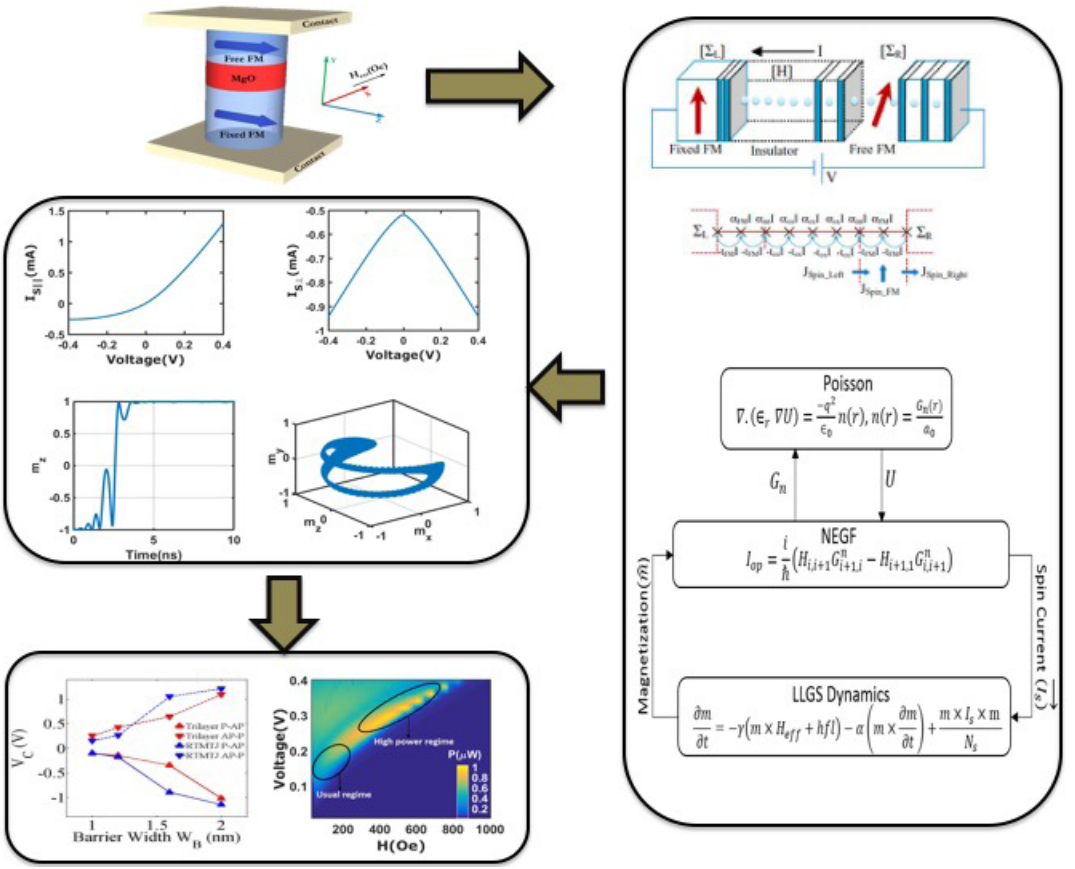
Multi-scale simulation studies on spin transfer torque magnetic tunnel junctions

Spin transfer torque magnetic random access memory (STT-MRAM) is a new memory technology based on electron spin. MRAM promises to bring non-volatile, low-power, low cost and high speed memory and has the potential to replace FLASH, DRAM and even hard-discs. The basic building cell of the STT-MRAM is the magnetic tunnel junction (MTJ) device. While STT-MRAM burgeons into a mature technology, explorations on magnetic tunnel junction (MTJ) device scaling pose an imminent need for a unified and predictive device simulation platform. A composite picture of the MTJ device functionality is a multi-dimensional problem where a viable device design necessarily requires the navigation over a very large and complex design landscape.



Capabilities of the simulation engine: a)-e) flow with arrow (a) Typical structure simulated includes the MgO barrier sandwiched between two ferromagnetic contacts b) typical schematic of the NEGF simulation platform. The barrier and the contacts are modeled atomically. A schematic also illustrates the simulation engine. Using this we generate the basic anatomy of an STT device which includes c) the torques, the switching characteristics and magnet trajectories. The analysis on these lines leads us to predict the device readability and reliability via switching voltage and power inferences.

A basic necessity here is a deeper understanding of spin transport across the structure, the physics of spin current absorption, the magnetisation dynamics of the free magnetic layer and the electronic properties of the interfaces. While there are basic simulators at each level, such as, *ab initio* magnetic materials design, micromagnetic simulations and basic interface chemistry, there is almost no effort to integrate the wisdom gained at each level.

Our group has advanced the development of a realistic simulator that combines spin-transport with interface chemistry and magnetisation dynamics. Such a combined platform will help us not only study current device designs under scaling by uncovering the basic anatomy of spin transfer torque from atomisitic principles, but will also facilitate the performance testing of viable device designs in the presence of imperfections such as roughness of interfaces and dephasing. This will facilitate a composite picture of the energy-delay-reliability trade-off of viable device designs starting from an atomistic picture.

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