IIT Bombay-SCL Technology Development

Sunny Sadana, Piyush Bhatt, Ashwin Lele Swaroop Ganguly, and **Udayan Ganguly**

Aug 17, 2018

For P. K. Patwardhan Tech Development Award

The IIT Bombay Team



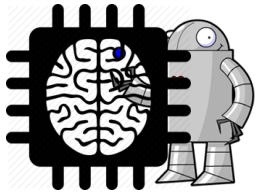


Why is Electronics Critical to India?

Electronics provides the solutions

Sensors & Internet of Things

High-Speed Communication



Big-Data & Computing

Green energy

Security & Encryption

Smart Living – City and Villages

Critical needs of India – "SHAPE"

Security

Healthcare

Agriculture

Pedagogy

Energy and Environment

Electronics is essential and ubiquitous

Secure Electronics is Critical

- Commercially India imports 100B USD/year. Strategic import is 10B/year and growing.
- National needs:
  - Strategic: Defence, Aerospace
  - Critical Infra: Smart Cities, E-commerce/Banking, Smart Agriculture, Secure Voting

Electronics is the new oil. India needs secure wells, then commercial ones.

Background & Motivation

- In 2011-12, Semi-Conductor Labs Chandigarh procured a 180 nm CMOS technology fabrication unit from Tower Jazz (Israel) for 1000s of Crores

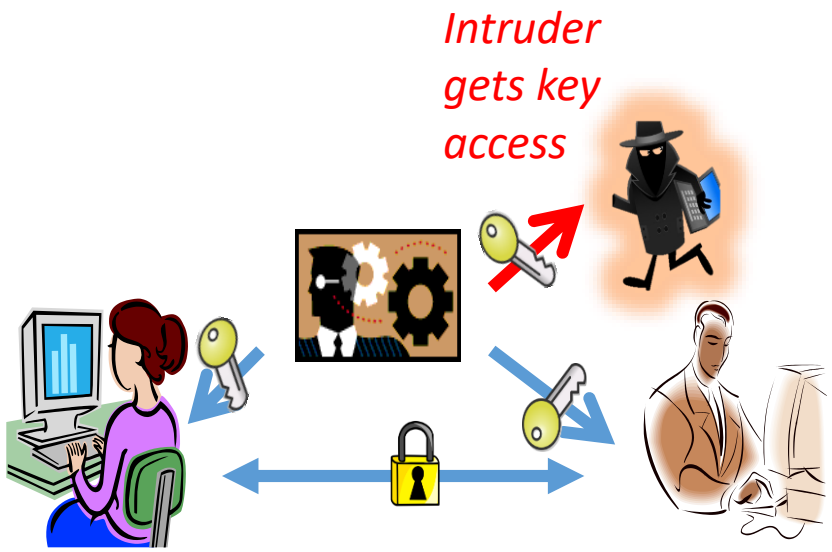
- **The challenge:** to address the major gaps in the offerings of the fab for high volume manufacturing (HVM)

1. BiCMOS technology (for RF based Radars & Communicat.)
2. One Time Programmable Memory (for code storage/secure memory e.g. electronic voting machines;)
3. Hardware Encryption for secure chips (e.g. banking, e-commerce etc.)
4. Multi-time Programmable Memory (for memory for secure India processor)

The goal is to develop strategic semiconductor technologies indigenously for HVM

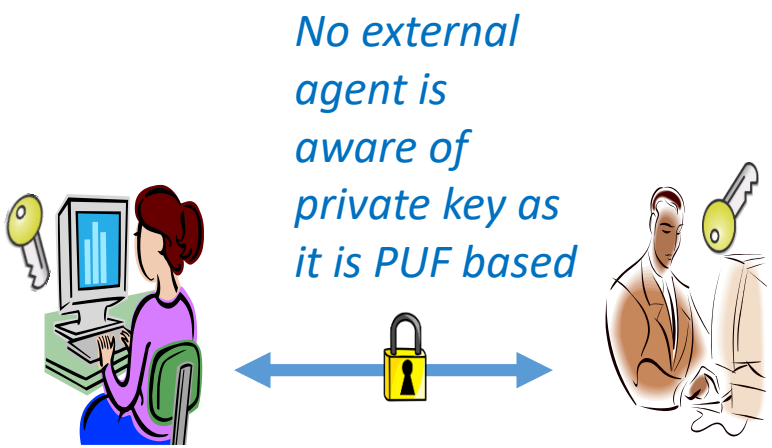
Security Key Risk vs. H/W key solution

- Soft ware keys are used for encryption/ authentication.
- These keys are generated by vendors or programs
- Accessible by govt./ operators etc.



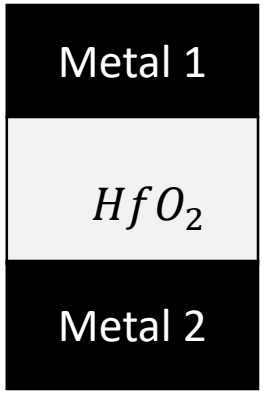
software encryption

- Solution: **A PUF based hardware key is such that**
- Key is **auto-generated internally** by the chip
- Mask independent i.e. same mask will produce random keys i.e. **"unique fingerprints"** the hardware
- **Unreadable** externally

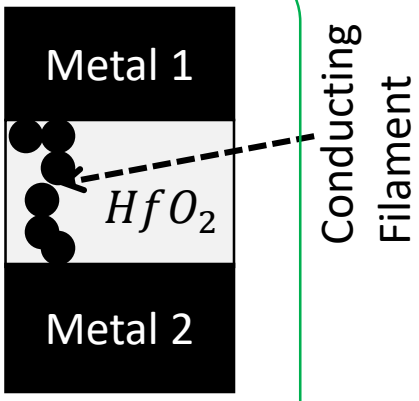


hardware encryption

OTP Technology Basics

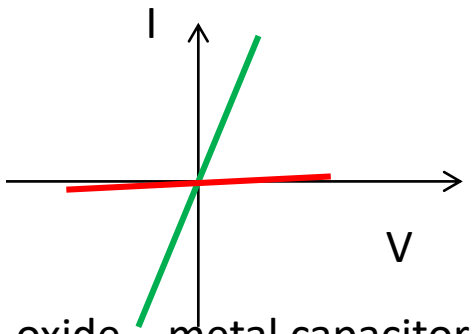


High resistance
before break down

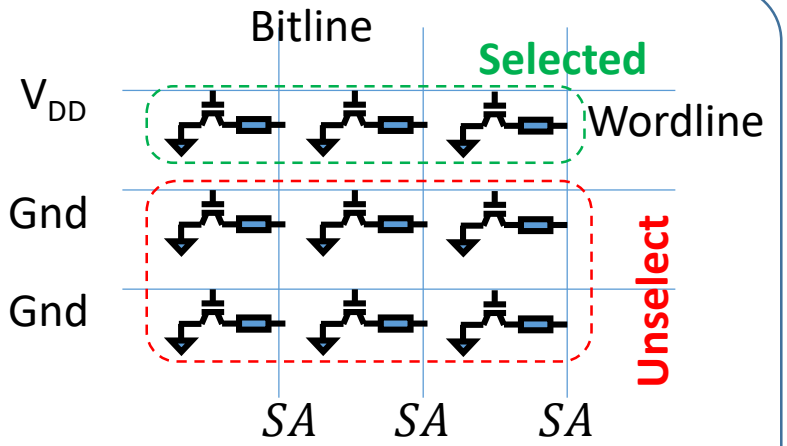


Low resistance
after break down

Breakdown process analog is lightening



A Metal – oxide – metal capacitor is used for 2 resistance states.



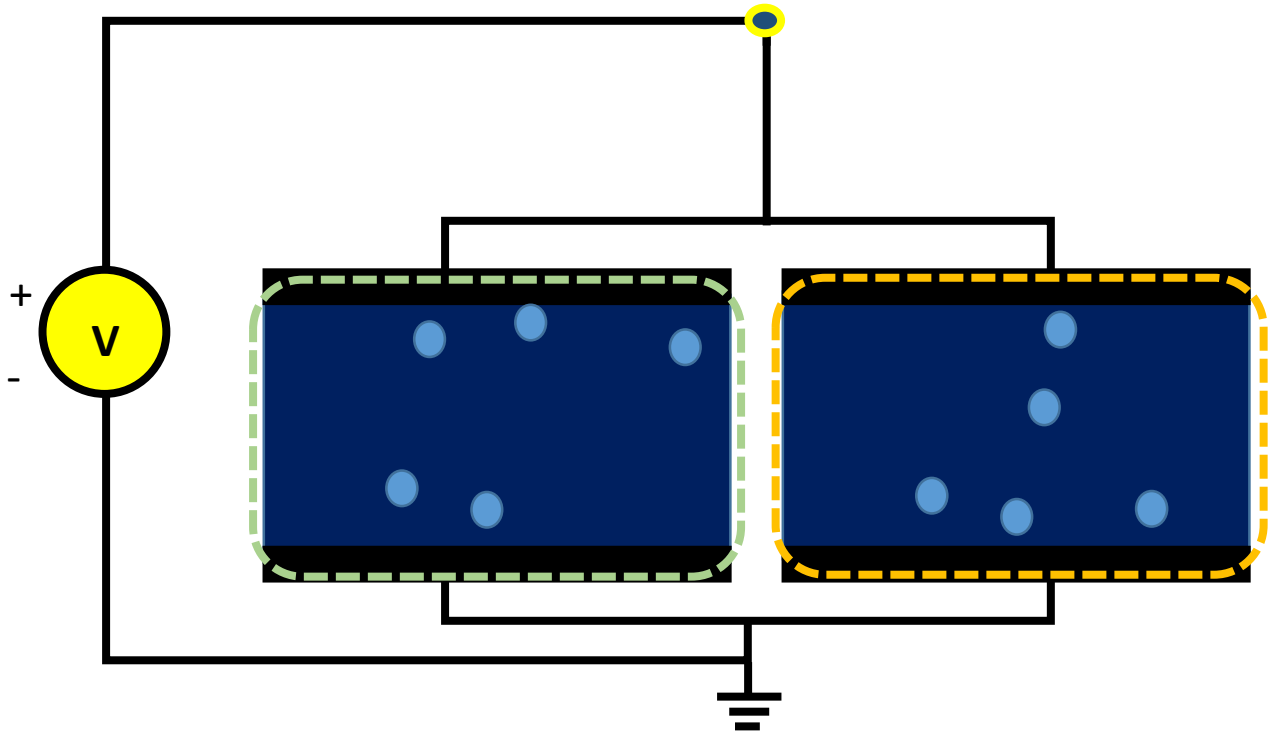
A simple array is made to read and write bits

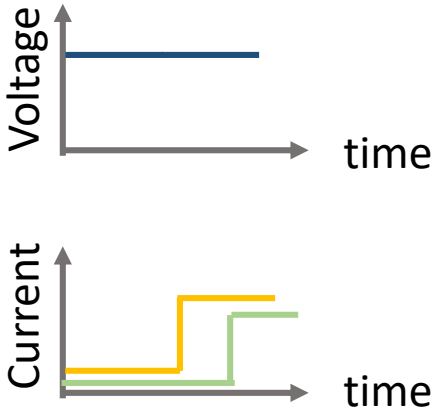
0101111000101010010 : Random bits

The challenge is (a) breakdown within supply voltage (3.3V)
(b) no further breakdown during operation (1.5V TDDB etc.)

Identical Metal Insulator Metal (MIM) Device

Both are macroscopically identical in size, shape and material,

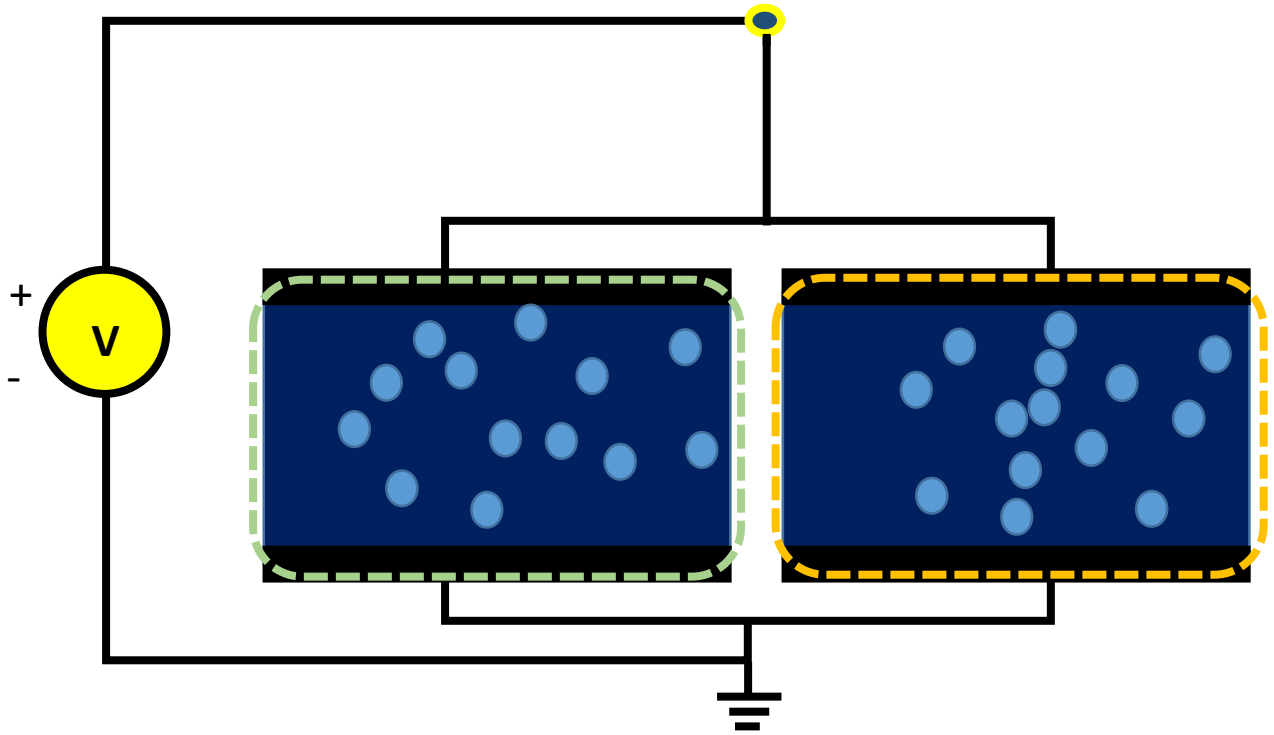


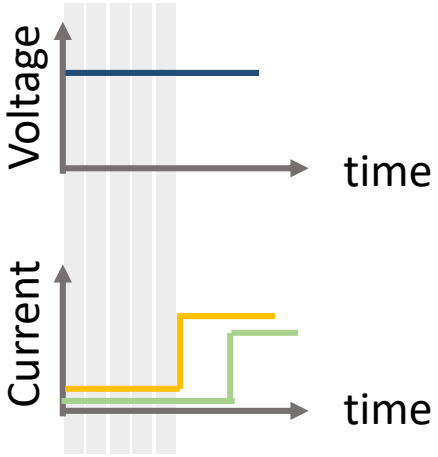


They have some initial atomic scale defects (e.g. missing atoms) – which are stochastic – hence **atomistically non-identical**

A Current Flow Generated Defects

If a voltage is applied, current flow.

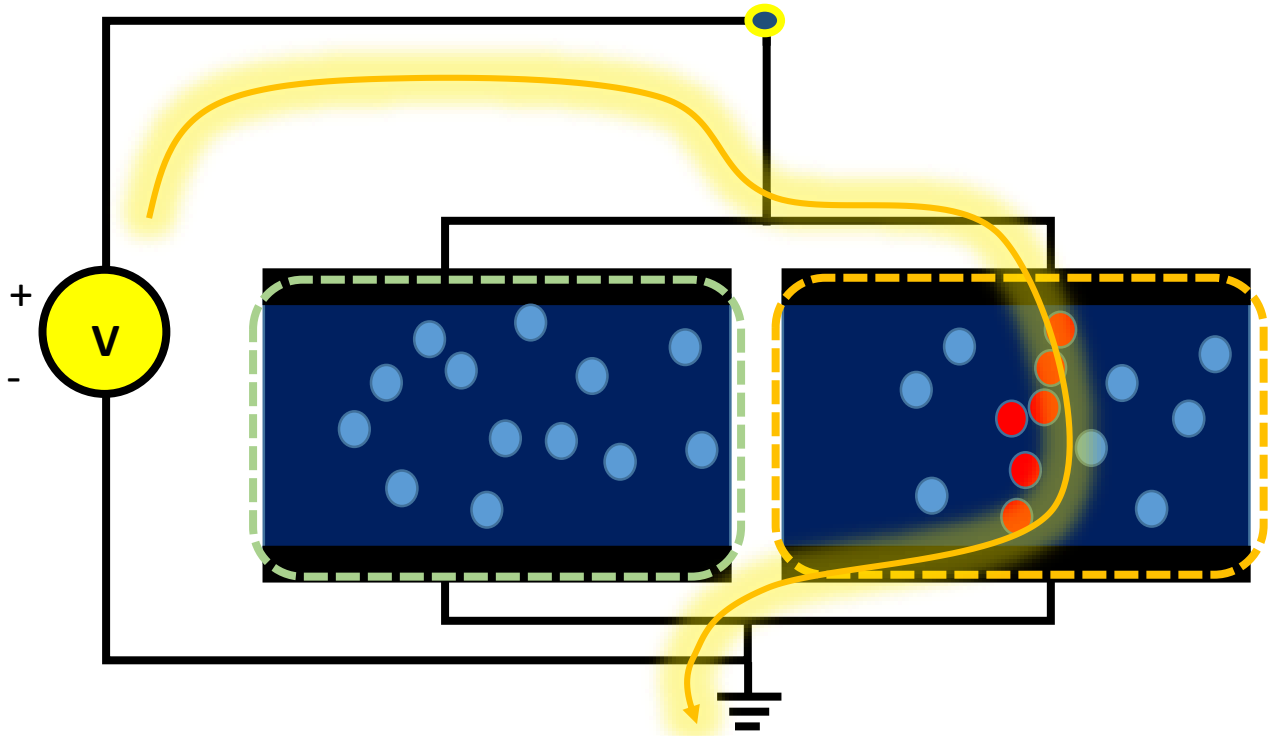


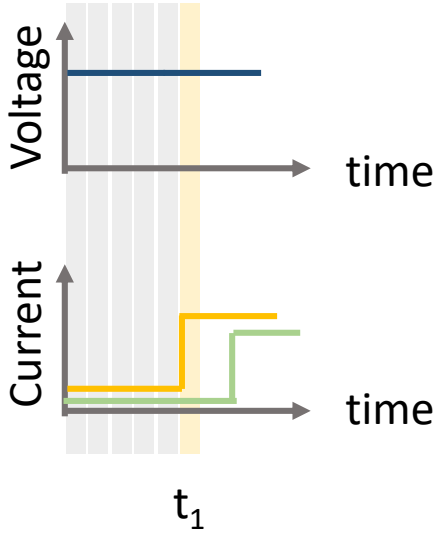


The electrons flowing through the oxide, it disturbs atomic arrangements further; some bonds break stochastically to dislodge atoms permanently to produce defects.

A conducting filament produces a short

When defects align to form a continuous path, a filament is formed.

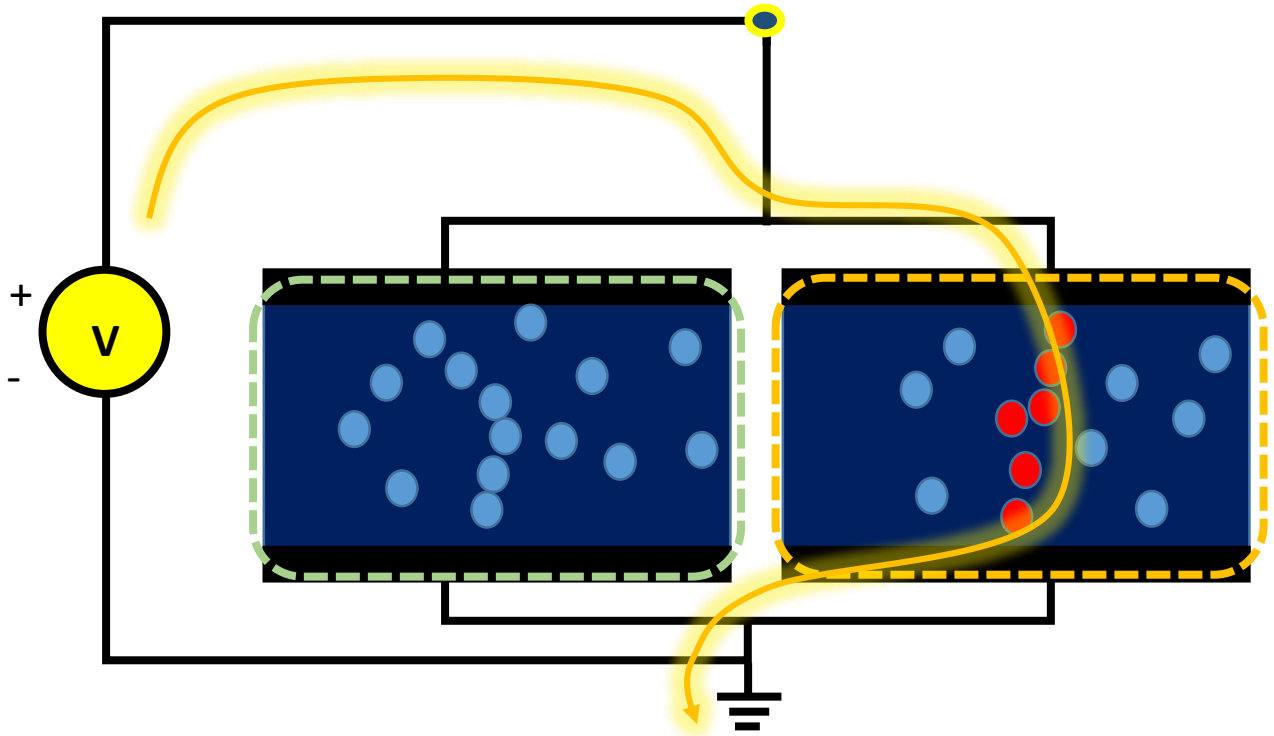


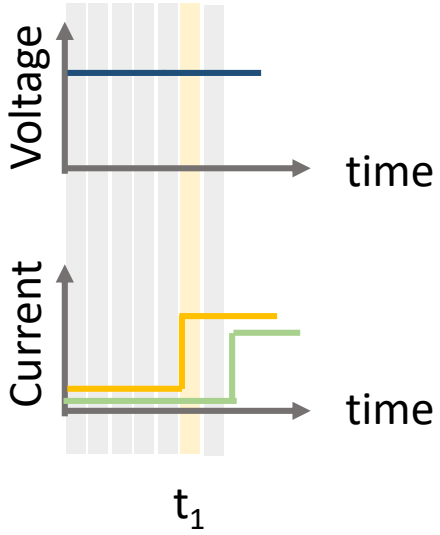


Suddenly, when the filament is formed at time t_1, the devices shorts and a large current flows; This is the low resistance state or logical “0”;

Two identical devices have different breakdown time

One device is short; but the other still is open circuit;

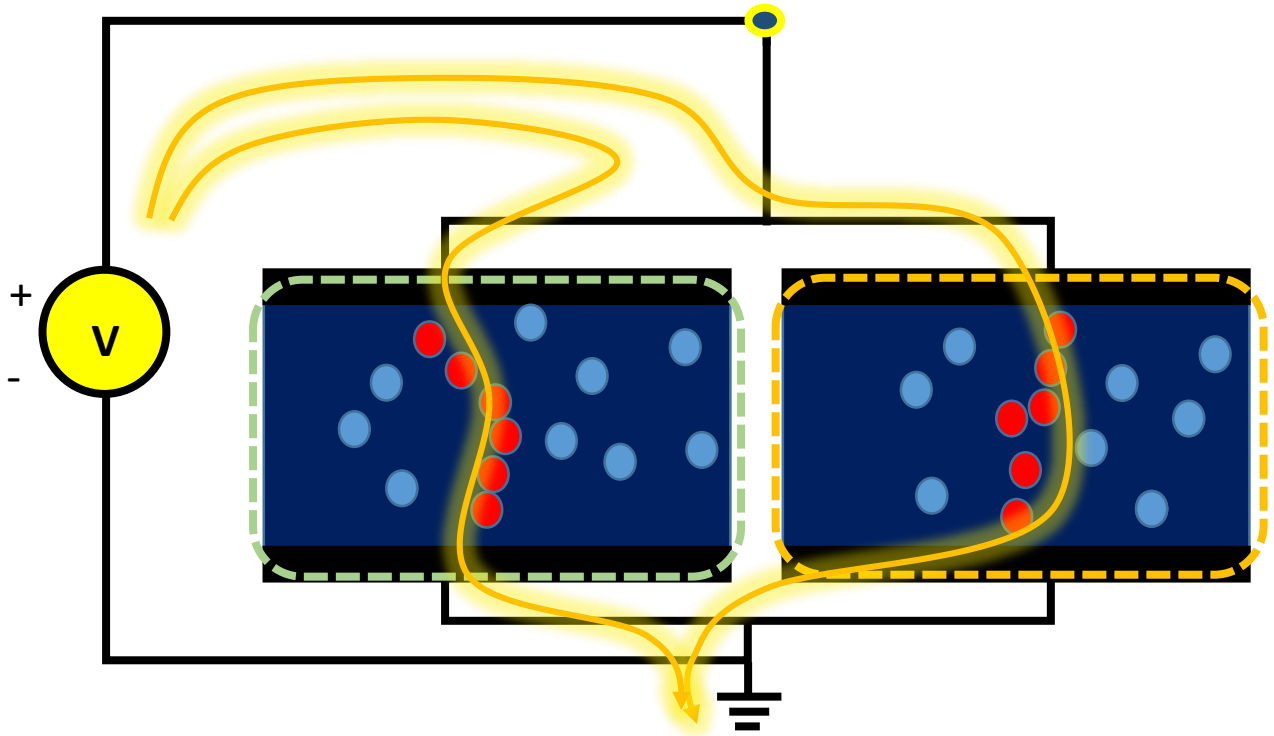


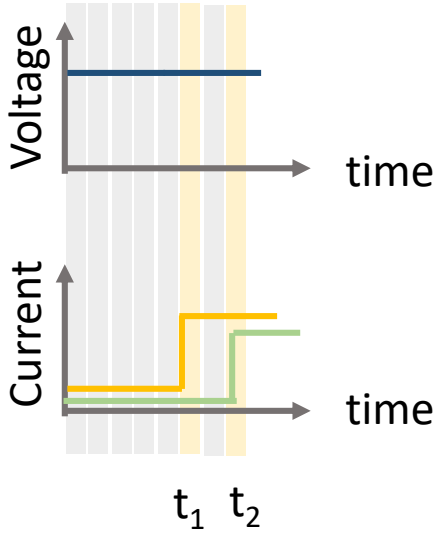


The other MIM devices needs to wait until is defects are generated such that a filament is formed.

Two identical devices have different breakdown time

One device is short; but the other still is open circuit;

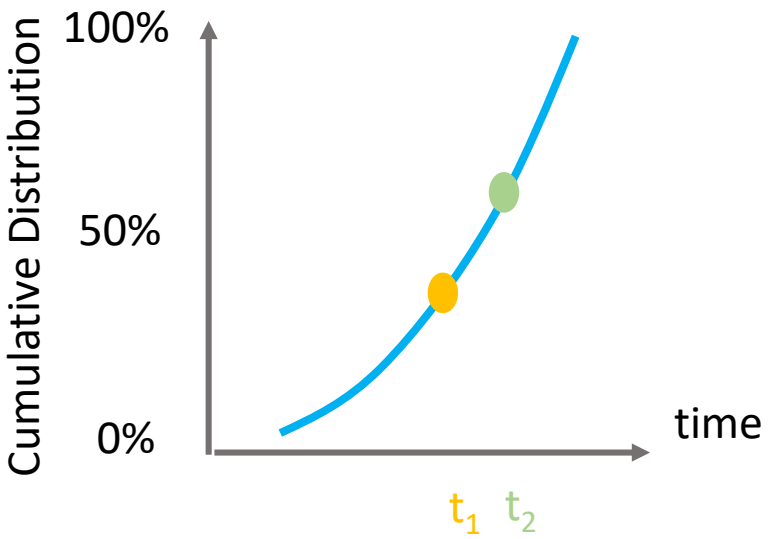


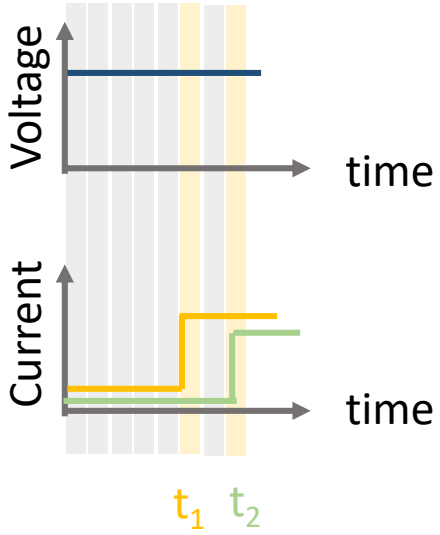


Eventually the second device will break down!

A distribution of breakdown time

When many (say 1000) devices are tested, each device breaks down at different times; For identical devices, the breakdown occurs at different times;

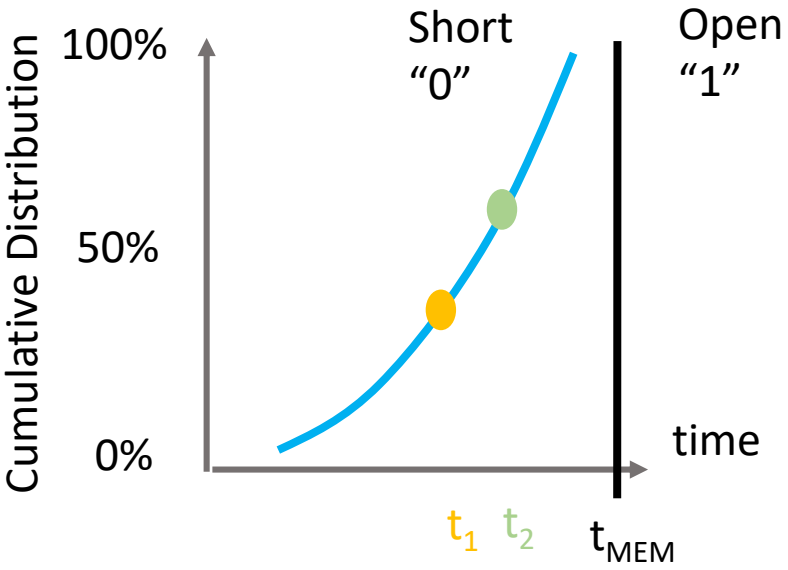


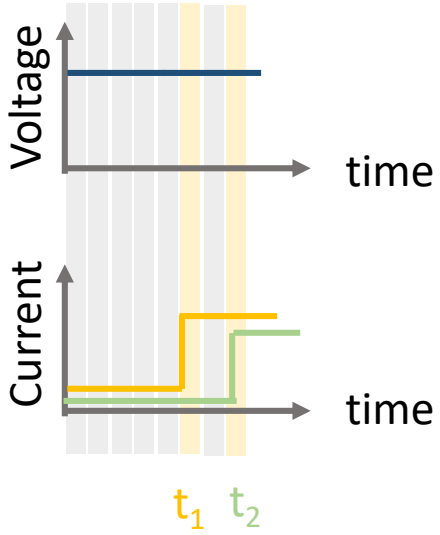


A cumulative distribution can be plotted;

Application 1: One Time Programmable Memory Technology

A memory technology requires that a MIM device be deterministically programmed to “0” ; Apply a high bias guarantees breakdown.



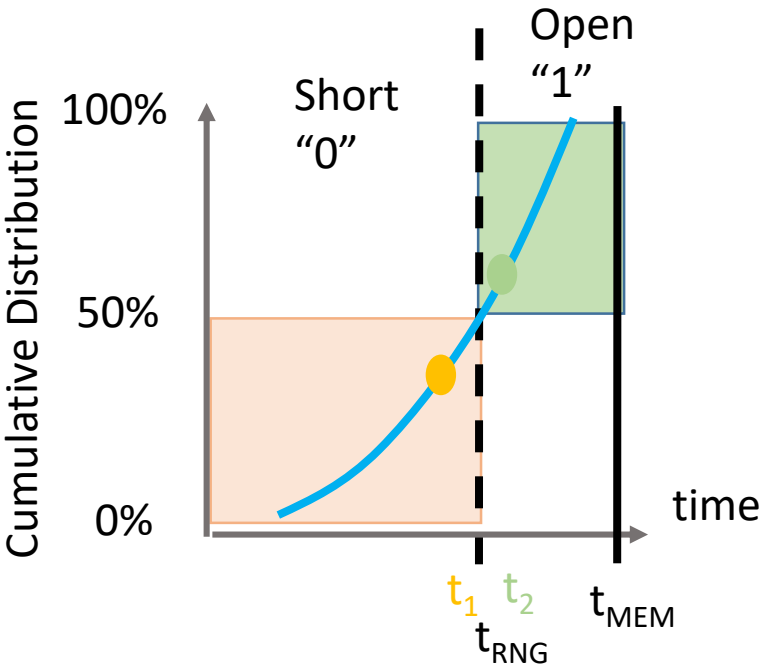


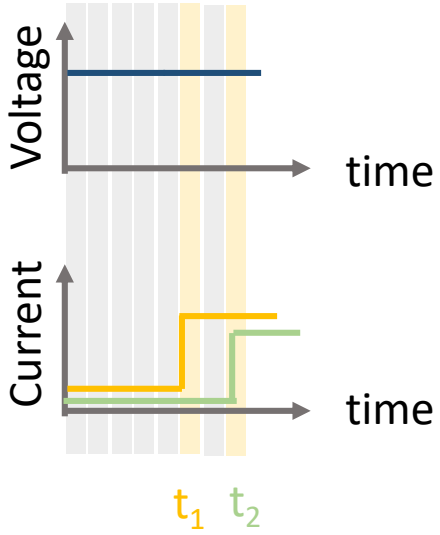
Given a $t_{pulse} = t_{MEM}$ where P=100%; then 100% is short (“0”);

Thus, we can program a bit with certainty!

Application 2: Physical Unclonable Function (PUF) Technology for chip ID

A chip ID requires a random barcode spontaneously generated (no one controls this) It is perfectly random; Hence completely unpredictable!



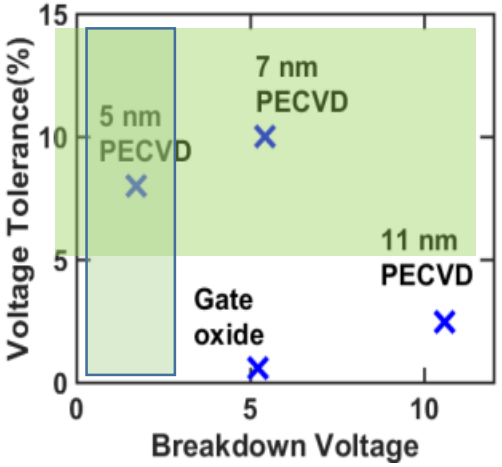


Given a $t_{pulse} = t_{RNG}$ where P=50%; then 50% devices will be open ("1") and 50% is short ("0"); However, it is impossible to guess, which ones.

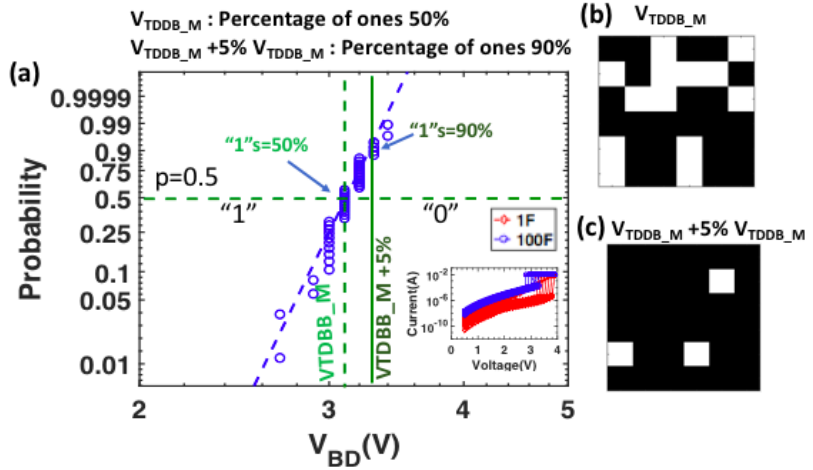
It's a Random Number Generator

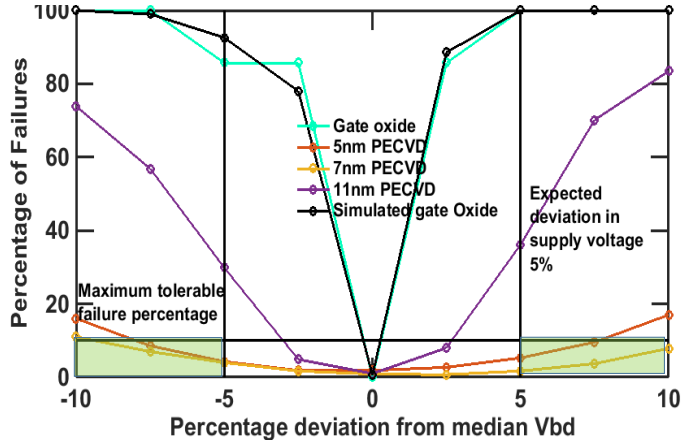
Lab Level Demo

A.Lele et al 75th DRC 2017; Indian Patent Appl. 2016



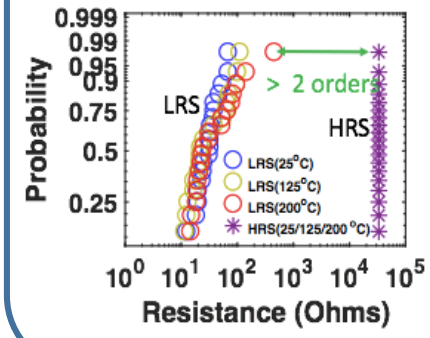
Lab level evaluation of VBD shows <3.3V VBD

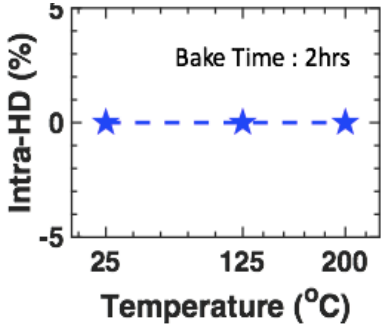




Challenge: Randomness / Uniqueness Lab is dependent V supply control (10%)

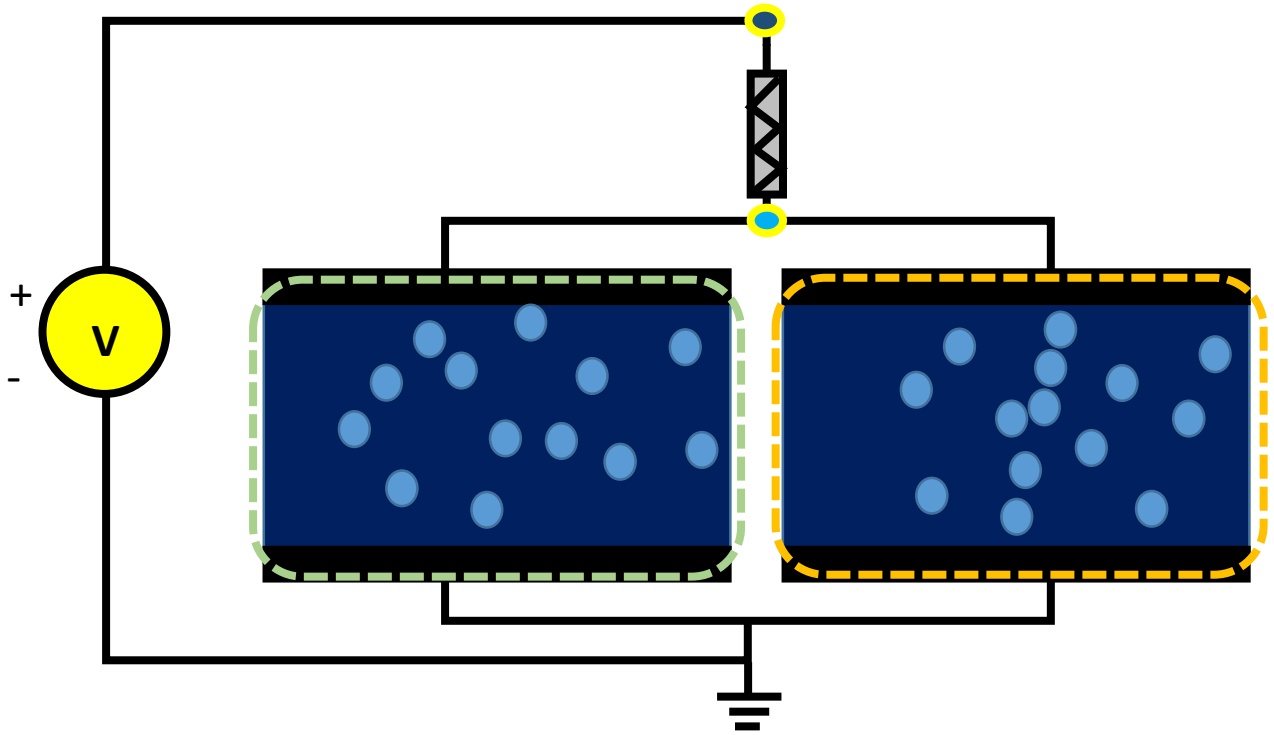
Lab level reliability is good

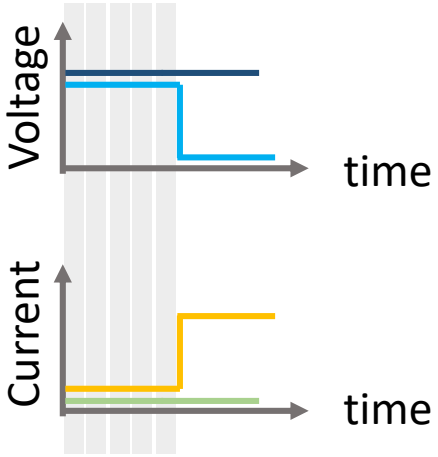




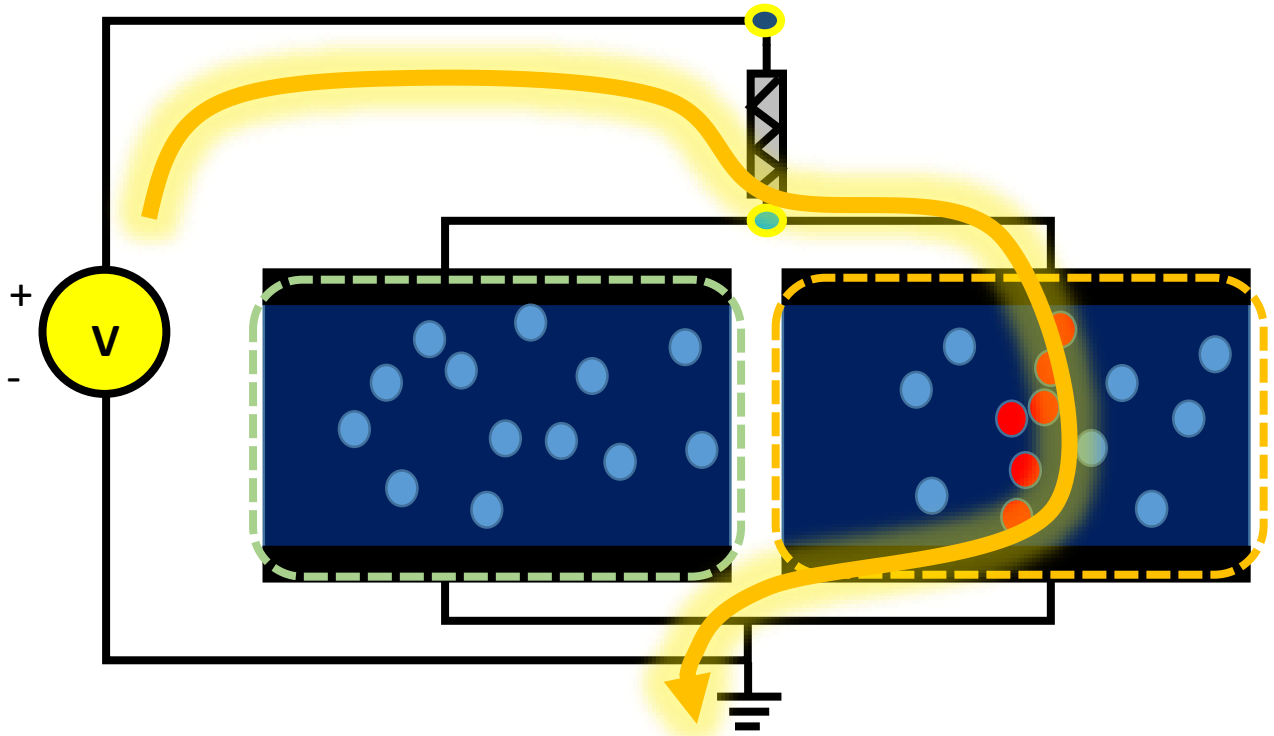
Specs are OK but V-supply variation is the critical challenge

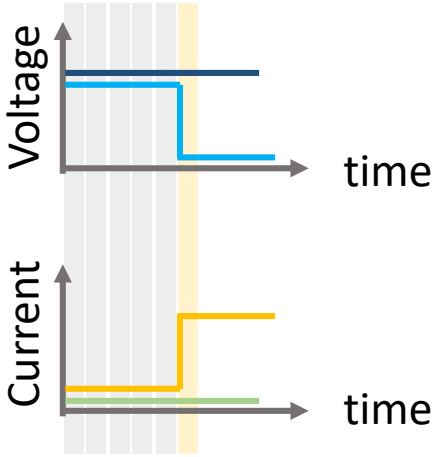
One Time Programmable Memory Technology



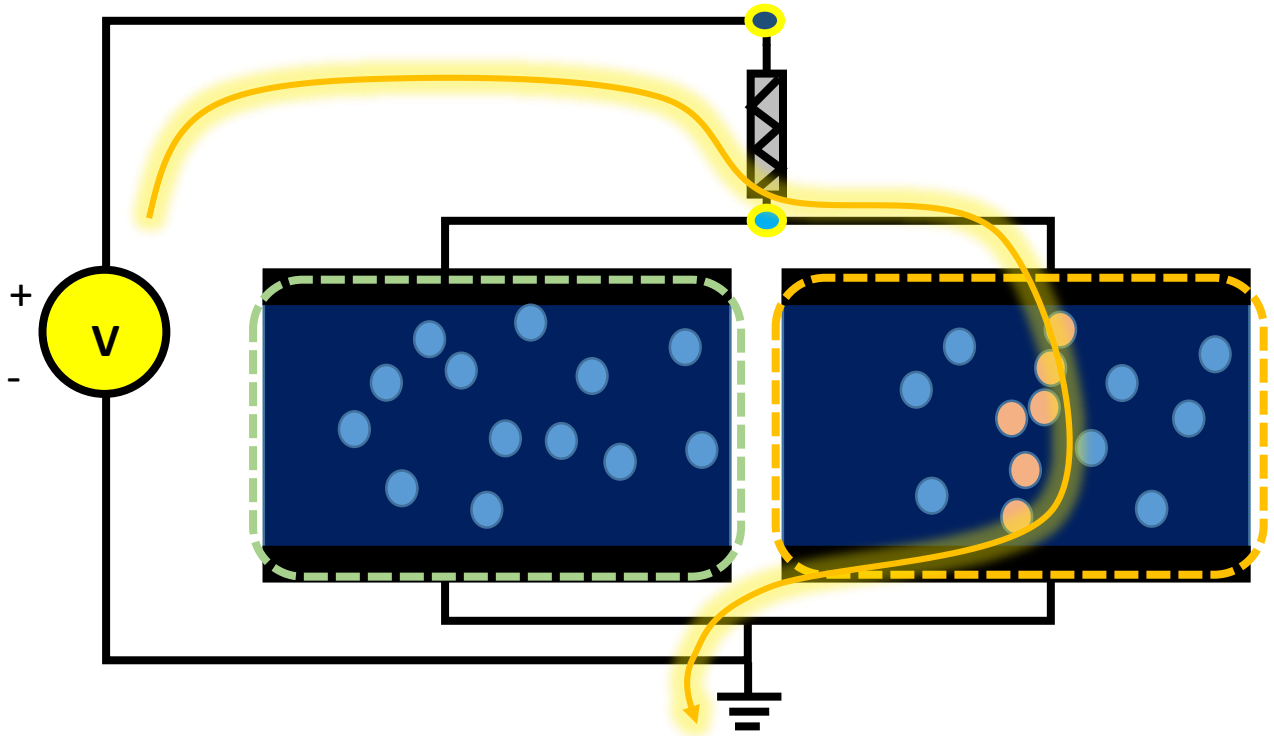


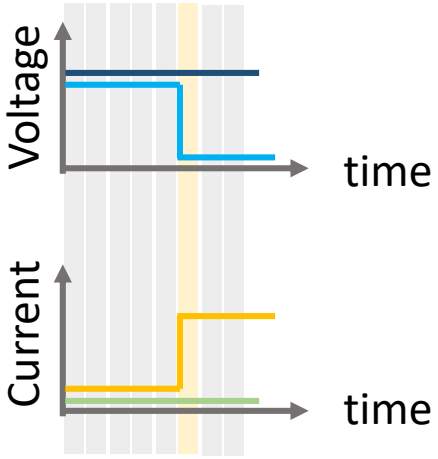
One Time Programmable Memory Technology



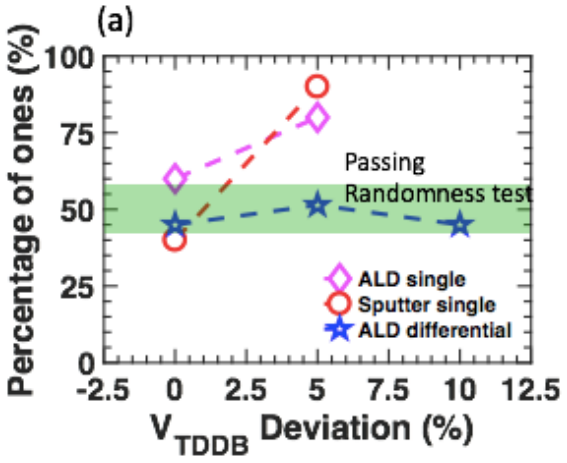


One Time Programmable Memory Technology



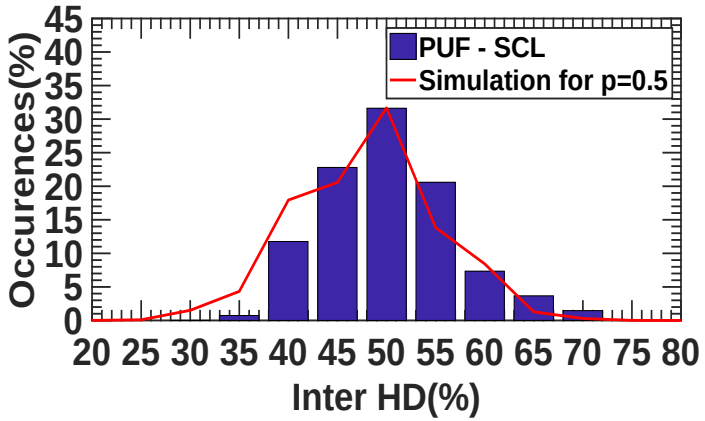


Tech 1: OTP & Tech 2: PUF Demonstration at SCL



V-supply variation tolerance

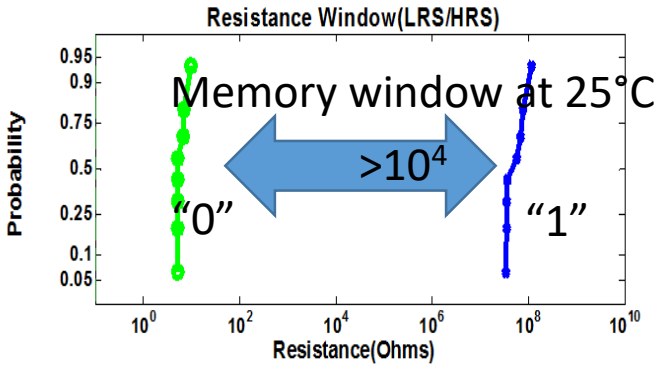
OTP PUF Tech.



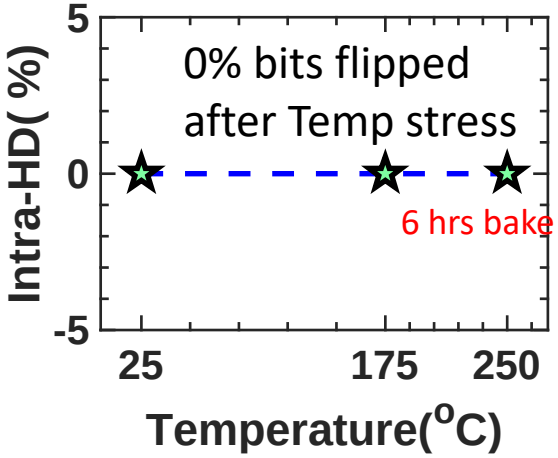
Perfectly stochastic (patent)

➔ Unbiased RNG

➔ NIST Tested



Memory States are digital



Extreme thermal stability

DRDO PUF ASIC

- Various specs

Team

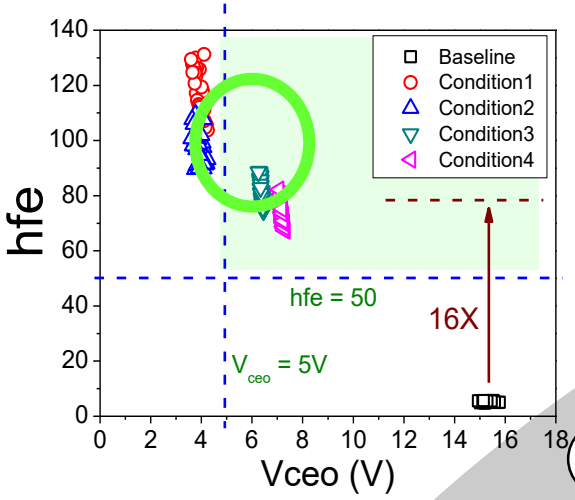
1. Fab (SCL)
2. Tech (IITB):
3. Circuit (IITD)
4. User (DRDO-PSA)

Achievement: Four Tech at 180 nm node in 2 years

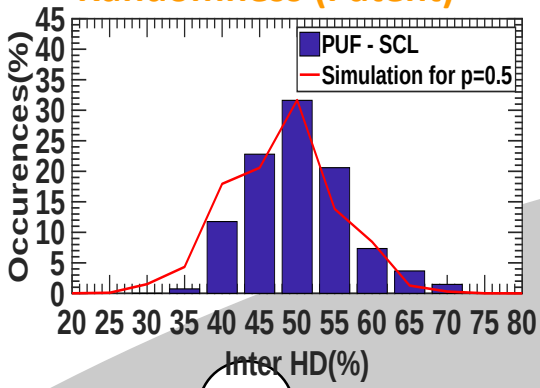
Demo in Manufacturing Fab

Plus 2 patents; 3 Conference; 1 Journal

BJT for BiCMOS



Perfect Unbiased Randomness (Patent)



Flash Memory

Excellent Performance & reliability

Hardware Encryption

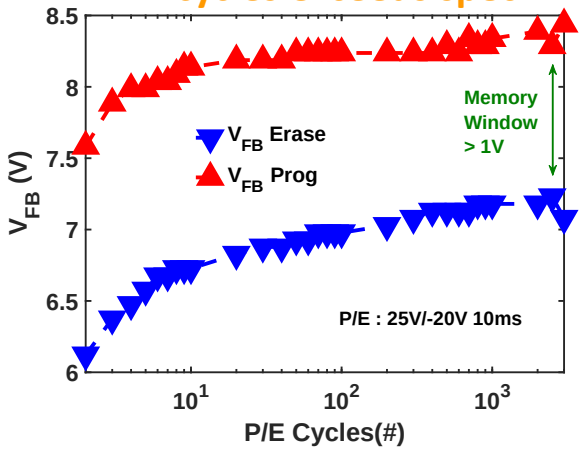
Perfectly stochastic h/w

➔ Unbiased RNG (cf. coin)

➔ NIST Test Passed

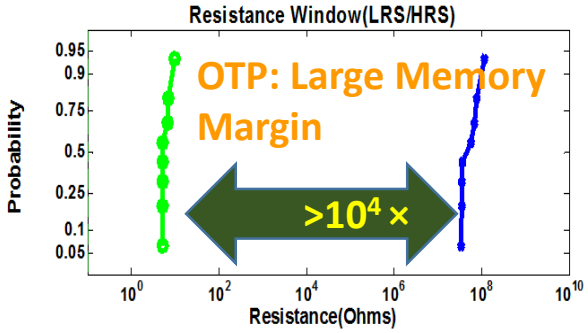
OTP Memory

Multiple (1000) cycles exceeds spec



Excellent Performance & reliability

BJT for BiCMOS



Experiments meet spec with 16x improvement

List of Impact

- July 2017: SCL has invited proposals from IITB on HBT Tech Dev (5 Crores)
- March 2018: IIT Bombay won a 50 Crore NNETRA proposal essential for CEN/IITBNF sustenance (2/4 deliverable related to IITB-SCL
- May 2018: ISRO Chairman Dr. Sivan has promised Tech Park engagement & ISRO-level committee to leverage in part IITB-SCL Tech Development
- Jun 2018: IIT Bombay is the coordinator for Strategic Nano-electronics @NNETRA
- Jun 2018: Principal Scientific Advisor's Office & DRDO has approved Encryption Chip Technology Project (5 Cr) with IIT B as Lead of a team of IITB-IITD-SCL-SETS
- Jun 2018: NITI Aayog Dr VK Saraswat requested a R&D Foundry proposal around national technology development lead by IIT Bombay (~1000 Crores)

Significant funding and focus from strategic agencies on IITB Nanoelectronics

IP and Papers

Patents

Two patents have been filed for OTP devices which is state of the art.

- U. Ganguly, S. Sadana, A. Lele, "**Method of generating controllably biased random number by OTP devices"** (Application No. 201821010427)
- P. Kumbhare, S. Sadana, U. Ganguly "**One Time Programmable Memory for Encryption and Reconfigurable Circuits""** (Application No. 201621031483)

Ideas are cutting edge concept published in top IEEE Conf & Journals

Publication

- S. Sadana, A. Lele, S. Tsundus, P. Kumbhare, U. Ganguly"**A Highly Reliable and Unbiased PUF based on Differential OTP memory**" IEEE Electron Devices Letters 2018
- Piyush Bhatt, Amit Kumar Singh, Monika Gupta, B.Umapathi, HS Jatana and U.Ganguly "**Technology development of CMOS compatible high gain BJT to enable 180nm BiCMOS technology"** International Workshop on The Physics of Semiconductor Devices (IWPSD 2017).
- S. Sadana, A. Singh, D. Sehgal, B. Umapathi, H.S. Jatana, U. Ganguly "**One Time Programmable (OTP) Memory based on MIM dielectric breakdown for 180nm CMOS**" International Workshop on The Physics of Semiconductor Devices (IWPSD) 2017.
- Lele, S. Sadana, A. Singh, H.S. Jatana, U. Ganguly "**A simple PECVD SiO2 OTP Memory based PUF for 180nm Node for IoT** " 75th Device Research Conference, 2017. link

Testimonials &News

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Department of Space, Government of India

Surinder Singh
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Dr. Udayan Ganguly,
Associate Professor ,
Dept of Electrical Engineering,
Indian Institute of Technology
Bombay

July 18, 2017

Subject: Collaboration between SCL and CEN at IIT Bombay

Dear Prof. Ganguly,

I would like to express my strong appreciation for the R&D at the Centre of Excellence in Nanoelectronics (CEN) at IIT Bombay and the progress of our collaboration with this Centre. Such a facility addresses key needs to technology development.

Secure Indigenous Chips Inbox x

Sudesh Kumar Vasudeva sudeshkumar.v@nic May 31
to head, me

Dear Prof Fernandes,

I would like to put on record our appreciation from the Office of Principal Scientific Advisor on the technology development lead by Prof Udayan Ganguly's team at SCL, Chandigarh.

Dr. S.K.Vasudeva
Scientific Consultant (Defence Technologies)
Office of the Principal Scientific Adviser to the Govt. of India
Tel. No. 011-23062738

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A made-in-India transistor that can make India's IoT technology a reality

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Spoorthy Raman
Oct 25, (Research Matters):

DH DECCAN HERALD

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Applications of a new semiconductor device

Spoorthy Raman, OCT 23 2017, 20:07PM IST | UPDATED: OCT 24 2017, 00:00AM IST

High-frequency circuits: Researchers have developed a BJT that can work with Bi-CMOS.

Strong appreciation from stakeholders and attention from media!

The Team & Acknowledgements

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The Semi-Conductor Labs Chandigarh Team

The IIT Bombay Team